IN THE CLAIMS:

Please cancel claims 1-7 in their entirety without prejudice nor disclaimer of the subject matter set forth therein.

Please add new claims 9-16 as follows.

8. (Original) A reset circuit which includes a plurality of asynchronous modules and a plurality of synchronous modules from a first state to a last stage for executing desired functions, and initializes each of the pluralities of asynchronous and synchronous modules arranged in a semiconductor integrated circuit, comprising:

input means for inputting a reset signal to initialize the plurality of asynchronous modules; and

pulse generation means connected to the input means to generate a reset pulse based on the reset signal, wherein:

the plurality of asynchronous modules include a first asynchronous module arranged at a first stage, which is connected to an output of the pulse generation means and receives the reset pulse to be initialized, and a second asynchronous module arranged at a next stage;

the first asynchronous module has first control means for generating a first reset signal to initialize the second asynchronous module, and outputting the first reset signal to the second asynchronous module after initialization in the first asynchronous module; and

the second asynchronous module has second control means which is connected to an output of the first asynchronous module, receives the first reset signal output from the first asynchronous module to be initialized, generates a second reset signal to initialize an asynchronous module arranged at a further next stage based on the first reset

signal from the first asynchronous module, and outputs the second reset signal after initialization in the second asynchronous module, the reset circuit further comprising:

clock input means for inputting a clock signal;

third control means connected to the second asynchronous module to output, upon detection of the second reset signal, a control signal corresponding to the second reset signal for a period until a last delayed reset signal is input for a synchronous module of a last stage; and

a plurality of delay means connected to the clock input means to delay an input signal in synchronization with the clock signal, and to output a delayed reset signal generated by the delaying, wherein:

the plurality of synchronous modules are connected corresponding to the plurality of delay means, operated in synchronization with the clock signal, and initialized in synchronization with the clock signal based on the control signal and the delayed reset signal; and

among the plurality of delay means, first delay means arranged at a first stage receives the control signal output from the third control means as the input signal, and each of second delay means arranged at stages thereafter receives the delayed reset signal output from delay means arranged at a previous stage as the input signal.

9. (New) A reset circuit embedded in a large-scale integrated circuit, comprising:

an input terminal which receives a reset signal of the large-scale integrated circuit from outside;

a pulse generation circuit connected to the input terminal, which generates a reset pulse signal by performing a logical operation with the reset signal;

a first module connected to the pulse generation circuit, wherein the first module comprises:

a first register connected to the pulse generation circuit, which is reset in response to the reset pulse signal; and

a first control circuit connected to the pulse generation circuit, which generates a first module reset signal by performing a logical operation with the reset pulse signal; and

a second module connected to the pulse generation circuit and the first module, wherein the second module comprises:

a second register connected the first control circuit of the first module, which is reset in response to the first module reset signal; and

a second control circuit connected to the pulse generation circuit, which generates a second module reset signal by performing a logical operation with the reset pulse signal.

10. (New) The reset circuit according to the claim 9, wherein the pulse generation circuit comprises:

a delay circuit connected to the input terminal, which delays the reset signal;

an inverting circuit connected to the input terminal, which inverts a potential level of the reset signal; and

an OR circuit connected to the delay circuit and the inverting circuit, which performs a logical OR operation with the delayed reset signal and the inverted reset signal, causing the reset pulse signal to be generated.

11. (New) The reset circuit according to claim 10, wherein the first control circuit of the first module comprises:

an AND circuit generating a clock signal by performing a logical AND operation with a plurality of initialization notification signals;

a flip-flop circuit connected to the pulse generation circuit, wherein the flip-flop circuit holds the reset pulse signal and outputs the held reset pulse signal on the basis of the clock signal;

a second delay circuit connected to the flip-flop circuit, which delays the output held reset signal;

a second inverting circuit connected to the flip-flop circuit, which inverts a potential level of the output held reset signal; and

a second OR circuit connected to the second delay circuit and the second inverting circuit, which performs a logical OR operation with the delayed output held reset signal and the inverted output held reset signal, causing the first module reset signal to be generated.

12. (New) The reset circuit according to the claim 9, wherein the pulse generation circuit comprises:

an inverting circuit connected to the input terminal, which inverts a potential level of the reset signal;

a delay circuit connected to the inverting circuit, which delays the inverted reset signal; and

an OR circuit connected to the input terminal and the inverting circuit, which performs a logical OR operation with the reset signal and the delayed inverted reset signal, causing the reset pulse signal to be generated.

13. (New) The reset circuit according to claim 12, wherein the first control circuit of the first module comprises:

an AND circuit generating a clock signal by performing a logical AND operation with a plurality of initialization notification signals;

a flip-flop circuit connected to the pulse generation circuit, wherein the flip-flop circuit holds the reset pulse signal and outputs the held reset pulse signal on the basis of the clock signal;

a second delay circuit connected to the flip-flop circuit, which delays the output held reset signal;

a second inverting circuit connected to the flip-flop circuit, which inverts a potential level of the output held reset signal; and

a second OR circuit connected to the second delay circuit and the second inverting circuit, which performs a logical OR operation with the delayed output held reset signal and the inverted output held reset signal, causing the first module reset signal to be generated.

14. (New) A reset circuit embedded in a large-scale integrated circuit, comprising:

an input terminal which receives a reset signal having a first and second potential levels;

a clock terminal which receives a clock signal;

a control circuit connected to the input terminal, which generates a signal having the second potential level when the reset signal having the second potential level is input until a second delay reset signal is input;

a first delay circuit connected to the control circuit and the clock terminal, which generates a first delay reset signal using the signal output from the control circuit in synchronization with the clock signal;

a second delay circuit connected to the first delay circuit and the clock terminal, which generates the second delay reset signal using the first delay reset signal in synchronization with the clock signal;

a first module connected to the first delay circuit, wherein the first module comprises a first register circuit which is initialized in synchronization with the clock signal and the first delay reset signal; and

a second module connected to the second delay circuit, wherein the second module comprises a second register circuit which is initialized in synchronization with the clock signal and the second delay reset signal.

15. (New) The reset circuit according to claim 14, wherein the control circuit comprises a set/reset type flip-flop having a first input terminal which receives the reset signal and a second input terminal which receives the second delay reset signal.

16. (New) The reset circuit according to claim 15, wherein the first register of the first module comprises:

an AND circuit performing a logical AND operation with the first delay reset signal and a data; and

a register connected to the AND circuit, which fetches the output of the AND circuit in synchronization with the clock signal.